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1/11/02**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .... 10/044,206  
Filing Date ..... January 11, 2002  
Inventor ..... Jerome Michael Eldridge  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2813  
Examiner ..... Laura M. Schillinger  
Attorney's Docket No. .... MI22-1914  
Title: Methods for Forming Void Regions, Dielectric Regions and Capacitor Constructions

**PRELIMINARY AMENDMENT A**

To: Assistant Commissioner for Patents  
Washington, D.C. 20231

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**AMENDMENTS****In the Specification**

At page 1, before the "Technical Field" insert the following:

**CROSS REFERENCE TO RELATED APPLICATION**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/651,815, filed August 30, 2000, entitled "Methods of Forming Void Regions, Dielectric Regions and Capacitor Constructions," naming Jerome Michael Eldridge as inventor, which is a continuation of U.S. Patent Application Serial No. 09/146,117, filed September 2, 1998, now U.S. Patent No. 6,140,200, the disclosures of which are incorporated by reference.